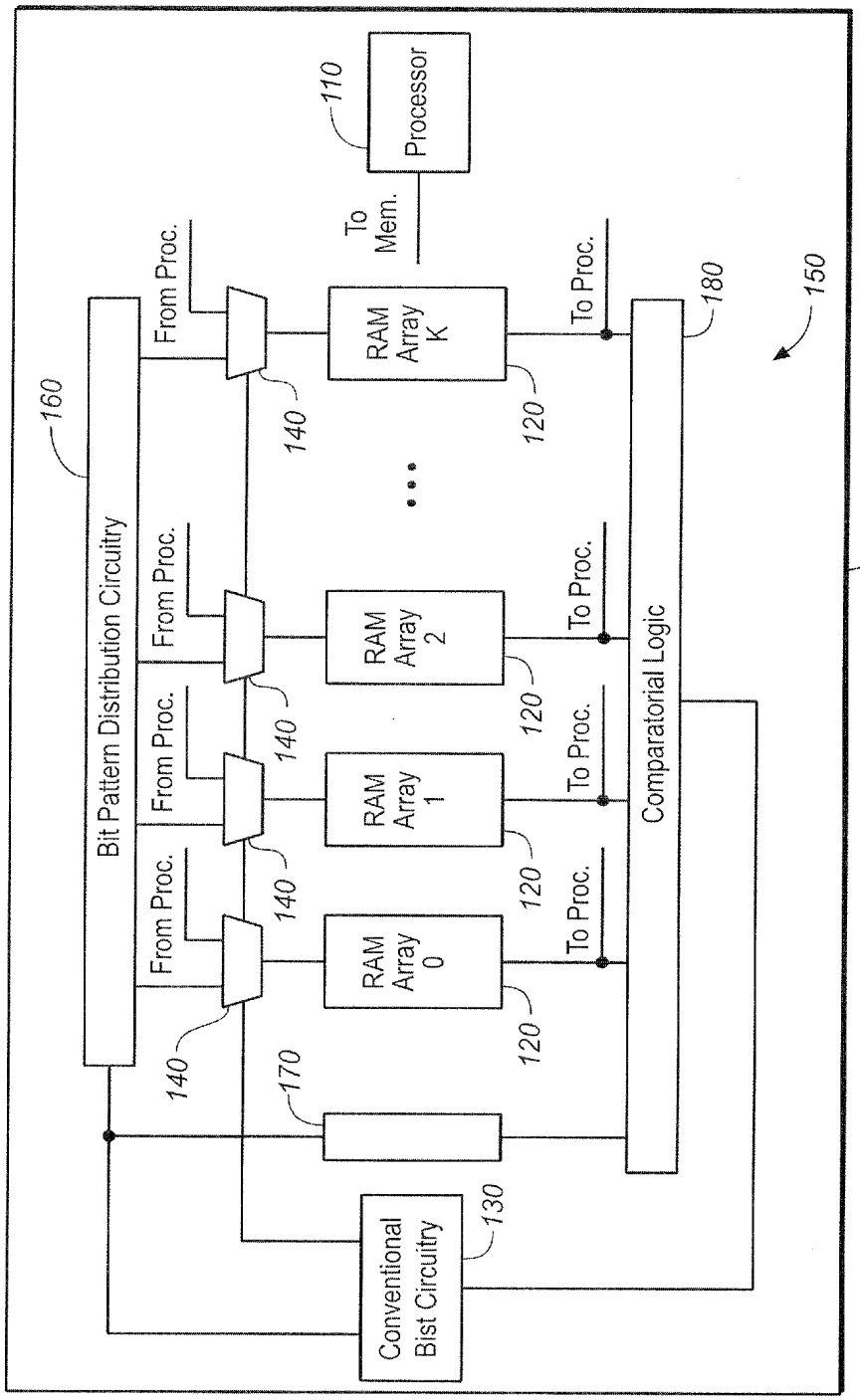
Processor
110
To Mem.
From Proc.
RAM Array K
120
140
To Proc.
180
150
160
Bit Pattern Distribution Circuitry
RAM Array 2
RAM Array 1
RAM Array 0
Comparatorial Logic
100
170
Conventional Bist Circuitry
130

FIG. 1

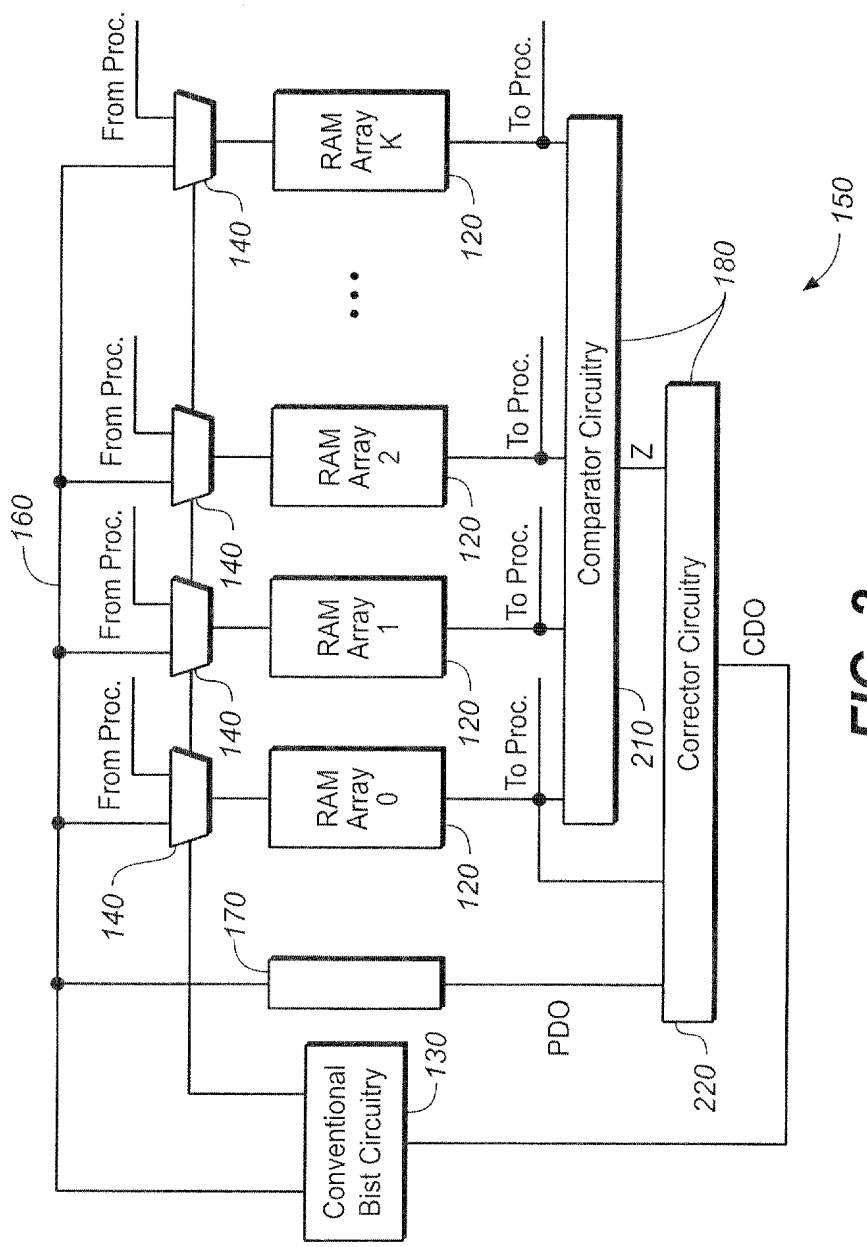
From Proc.
From Proc.
From Proc.
From Proc.
140
140
140
140
RAM Array K
RAM Array 2
RAM Array 1
RAM Array 0
120
120
120
120
To Proc.
To Proc.
To Proc.
To Proc.
Comparator Circuitry
Z
180
150
160
210
Corrector Circuitry
CDO
170
PDO
220
Conventional Bist Circuitry
130

FIG. 2

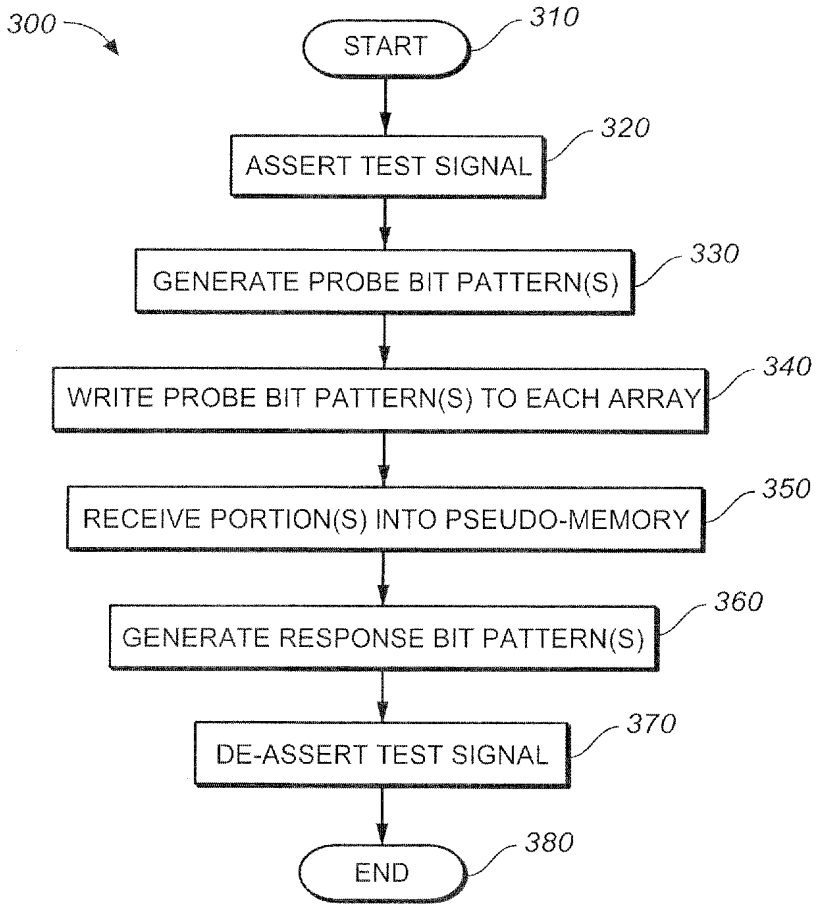
300
START
310
ASSERT TEST SIGNAL
320
GENERATE PROBE BIT PATTERN(S)
330
WRITE PROBE BIT PATTERN(S) TO EACH ARRAY
340
RECEIVE PORTION(S) INTO PSEUDO-MEMORY
350
GENERATE RESPONSE BIT PATTERN(S)
360
DE-ASSERT TEST SIGNAL
370
END
380

FIG. 3